1.4μW/channel 16-channel EEG/ECoG Processor for Smart Brain Sensor SoC

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Abstract

A 16-channel smart brain sensor SoC is proposed with the integrated digital EEG/ECoG processor (DEEP) to perform multi-dimension feature space analysis algorithms. The DEEP has three processing pipelines to filter out the artifacts, extract the multi-domain features, and interpret the inherent meanings according to the applications. Dedicated accelerators as well as a RISC are embedded to provide efficient computation and flexibility. Processing folding among channels saves the dominating leakage power. 1.4μW/channel power is achieved after the implementation in 90nm process.

Introduction

Biomedical sensors equipped with online physiological-signal feature analysis (PFA) processor can enhance applications such as responsive neurostimulation (RNS), brain computer interface, ambulatory monitor with vital sign detection, body sensor network, etc. The VLSI hardware is attractive because of the power and area constraints imposed by the portable and implantable requirements. Although many advanced PFA algorithms have been proposed and the micro-watt multi-channel signal acquisition circuitry has been designed [1], only basic analysis tools are implemented on-chip for few recording channels [2-3]. In this paper a 16-channel smart brain sensor (SBS) is designed by integrating a digital electroencephalogram (EEG)/electrocorticogram (ECoG) processor (DEEP) with the analog signal acquisition circuitry (ASAC). In the proposed DEEP, the PFA procedure shown in Fig. 1 is efficiently mapped into a three-stage pipelined structure. Dedicated processing units, reconfigurable logics, and a reduced instruction set computer are jointly utilized to provide the intensive computation as well as the flexibility. Multi-domain features are extracted for multiple channels for more accurate analysis. The interpretation of the features can be programmed according to the application requirements. The processing response can be as short as 0.1sec for the real-time constraint. 1.4μW/channel power is achieved by realizing the advanced architecture in 90nm process.

Digital EEG/ECoG Processor

Figure 2 shows the proposed DEEP. The PFA of brain signals is composed of three sequential stages: pre-processing (PP), feature extraction (FE), and classification and decoding (CD). These stages are mapped into three processing pipelines with heterogeneous hardware units reflecting the needs on each stage. The PP pipeline performs the temporal and spatial linear filtering with dedicated parallel processing units. The recorded brain signals are usually contaminated with artifacts such as 60Hz power-line noise, electrooculography, and electromyography signals. In addition the information of interest may be located at a specific frequency band (i.e. alpha wave for sleep detection), or scattered over multiple recording sites for a specific brain task (i.e. motor imagery). Therefore, the filters are used to remove the artifact and assemble the signal-of-interest. The filter coefficients could be programmed after the offline calibration with the training algorithms such as spectral analysis, independent component analysis, and common spatial pattern. The filtering of raw data for multiple channels requires large computation with a regular schedule. Multiplication and accumulation (MAC) units are thus cascaded with register arrays to save significant memory-access power required by the general purposed processor.

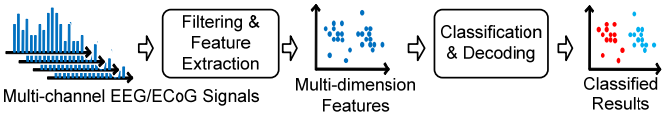

Fig. 1. Procedure of Physiological-signal Feature Analysis.

Multiple feature extraction units combined with a MAC unit are utilized on the FE stage. One of the main difficulties to provide a flexible PFA processor is that the biomarkers may be hidden in different physical domains for various applications and testing subjects. Utilizing the multiple features could increase the accuracy of the applications, enhance the robustness over the variety, and envision the discovery of more properties about the brain dynamics. Four kinds of features are extracted in parallel for 16 channels, including temporal-domain characteristics, spatial-domain cross-channel correlations, frequency-domain spectrum features, and nonlinear chaotic values. After the feature extraction, the MAC unit reduces the dimension of the feature space with the offline training algorithm such as principal component analysis. Dedicated accelerators and reconfigurable logics are jointly utilized on this stage to provide efficient computation and sufficient flexibility. For example the temporal characteristics such as energy, variance, and so on are calculated by ALUs according to the hardware configuration. The spectrum analysis is accelerated by a dedicated fast Fourier transformation (FFT) unit followed by the reconfigurable ALUs.

The CD has less requirement on computation and memory because of the reduced data amount after the FE. A reduced instruction set computer (RISC) is embedded to preserve fully programmability for the CD algorithms that generally have complicated and sequential processing schedule. The program counter of the RISC is activated by the FE pipeline af-

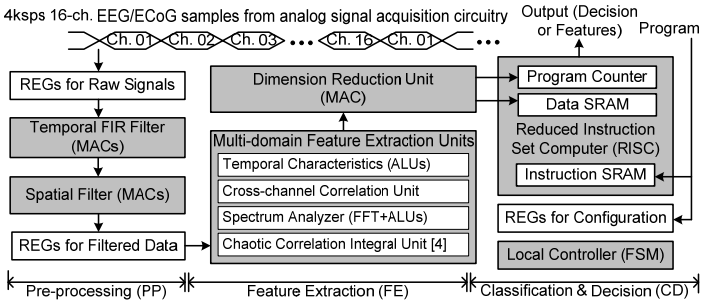

Fig. 2. Architecture of the proposed digital EEG/ECoG processor.

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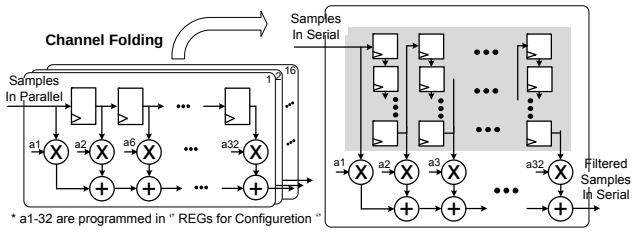


Fig. 3. Processing folding among multiple channels to save area and the corresponding leakage power.

ter the extracted features are fed forward to the specific addresses in the data memory. The chip output could be the extracted features or the decision results according to the program. As for the throughput, the PP pipeline keeps passing the raw samples cycle by cycle while the FE is scheduled to have 10 processing iterations for each second. Therefore, the decision can be made every 0.1 sec in maximum for the realtime applications.

Since the processing procedures are identical for 16 channels, processing folding among multiple channels is utilized to save area and power. An example is shown in Figure 3 for temporal filtering in the PP pipeline. Sixteen rows of registers are cascaded to propagate the raw data of 16 channels. A single of the parallel processing core is used to sequentially perform filtering for 16 channels with a sophisticated schedule. 78% area and 0.22µW/channel leakage power are saved compared with the architecture using 16 filters. As for FE pipeline, 68% area and 2.38µW/channel power are saved after the channel folding.

Analog Signal Acquisition Circuitry

Figure 4 shows the integrated 16-channel ASAC. One set of the programmable gain amplifier (PGA), chopper, low-pass filter (LPF), and SAR-ADC is shared by 16 chopper-stabilized low-noise amplifiers (LNAs) with an analog MUX [1,5]. Compare with duplicating a single channel 16 times, 16.94mm^2 is saved. Meanwhile 16 LNAs are turned on alternately to save power. The LNA employs the current-mode instrumentation amplifier for 1V operation and capacitor-coupled input stage for eliminating the electrode-tissue offset voltage. The AC-coupled high-pass corner is tunable from 0.1Hz to 1Hz. A 40dB gain is provided by LNA while the PGA offers an additional 6dB to 40dB programmable gain. A 3rd-order elliptic Gm-C LPF following the PGA removes the noise modulated to the chopper frequency at 10kHz.

Implementation Results

The die micrograph and chip specifications are shown in Fig. 5. The 16-channel smart brain sensor SoC consumes 14.8mm^2 area and 14.4µW/channel power. The integrated DEEP consumes 2.1mm^2 and 1.4µW/channel with 231k logic gates and 64.1kb SRAMs. Comparison of the on-chip pro-

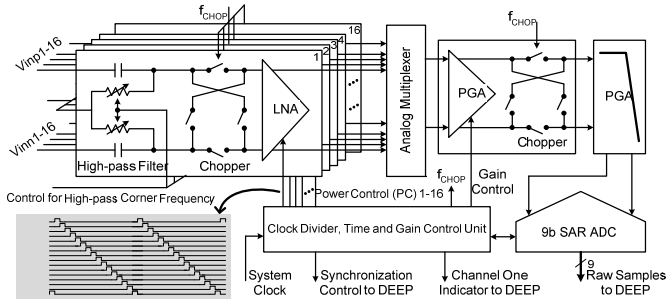
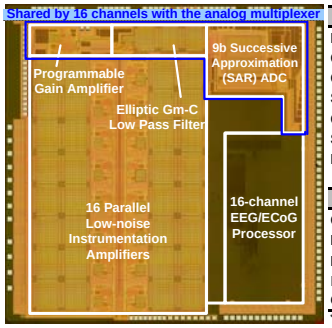


Fig. 4. 16-channel analog signal acquisition circuitry (ASAC).



Specifications of Smart Brain Sensor Chip	
Process	90nm Low Leakage CMOS
Chip Area	14.82 (3.8 x 3.9) mm^2
Core Area	11.94 mm^2
Supply Voltage	1.0V
Channel Number	16
System Clock	49.15kHz
Power Consumption	ASAC: 10.31µW /Channel *
	DEEP: 1.41µW /Channel **
Digital EEG/ECoG Processor (DEEP)	
Core Area	2.1mm^2
Logic Gate	231k
Memory	64.1kb (25.52% Core Area)
Input Signals	16Ch., 256sps/ch., 9b/sample
Operation Frequency	4.096kHz

** Measured result * Simulated result

Fig. 5. Architecture of the proposed digital EEG/ECoG processor.

Table. 1. Comparison of the on-chip EEG/ECoG processors

	Process	Area/Ch. (Processor Only)	Power/Ch. (Processor Only)	Key Processing Features	Ch. Num.	Processing Iteration	SoC Integration
[6]	0.8µm	5mm^2	4.5µW	Analog spectrum analysis processor	4	5Hz	Amp.
[3]	0.13µm	16mm^2 (SoC)	95µW (1MIPS)	General purpose processor + MAC	1	n/a	Amp.+ADC
[2]	0.18µm	2.92mm^2	2.1µW	Band-pass filters + energy accumulator	1	0.5Hz	Amp.+ADC
This Work	90nm	0.13mm^2	1.4 µW	PP: Temporal FIR filter, spatial linear filter FE: Temporal characteristic ALU, spectrum analysis unit, cross-channel correlator, correlation interal unit, MAC unit for dimension reduction CD: Programmable RISC	16	10Hz	Amp.+ADC

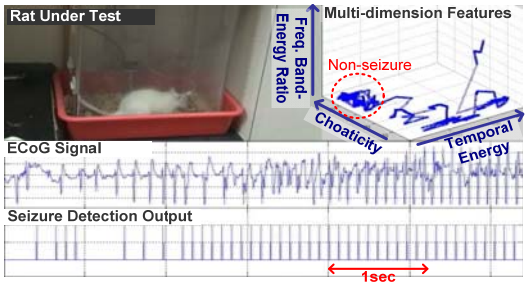


Fig. 6. Seizure early detection with DEEP for RNS on the rat.

cessors for bio-signal analysis is summarized in Table 1.

Seizure Early Detection with DEEP for RNS

RNS is the emerging therapy to control the epilepsy. RNS interrupts the epileptic seizure by sending the electrical stimuli into the brain before the seizure onset. Figure 6 demonstrates that the DEEP analyzes the ECoG and detects the early stage of a chemically-induced seizure for the rat. The decreased brain chaoticity, the increased temporal energy, and the oscillation frequency of the rhythmic discharge were observed sequentially on the feature space. The on-chip RISC performed the fast K nearest neighbor algorithm [7] in a real time to activate the stimulator once the seizure is detected.

References

[1] R. F. Yazicioglu, , et al., "A 200µW Eight-Channel Acquisition ASIC for Ambulatory EEG Systems," *ISSCC Dig. Tech. Papers*, pp. 164-603, Feb. 2008.

[2] N. Verma., wt al., "A Micro-power EEG acquisition SoC with integrated seizure detection processor for continuous patient monitoring," Symp. on VLSI Circuits, pp 62-63, June 2009

[3] A. C.-W. Wong, , et al., "A 1V, Micropower System-on-Chip for Vital-Sign Monitoring in Wireless Body Sensor Networks," *ISSCC Dig. Tech. Papers*, pp. 138-602, Feb. 2008.

[4] Yu-Hsin Chen, , et al., "Sub-microwatt Correlation Integral Processor for Implantable Closed-loop Epileptic Neuromodulator," to appear, *Int. Symp. on Circuits and Syst.*, May 2010.

[5] R. R. Harrison, et al., "A Low-Power Integrated Circuit for a Wireless 100-Electrode Neural Recording System," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 123-133, 2007.

[6] A. T. Avestruz, , et al., "A 5 µW/Channel Spectral Analysis IC for Chronic Bidirectional Brain-Machine Interfaces," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 3006-3024, Dec. 2008.

[7] Yu-Hsin Chen, et al., "Sub-microwatt KNN Classifier for Implantable Closed-loop Epileptic Neuromodulation System," *Int. Symp. on Bioelectron. and Bioinf.*, Dec. 2009